WHAT IS CLAIMED IS:

1. A method for predicting performance of an integrated circuit in an early stage of development, comprising:

a first step of obtaining respective performances of different types of first and second circuits in accordance with an existing generation process;

a second step of obtaining a performance correlation coefficient between the first and second circuits; and

a third step of predicting, using a predicted value or a target value for performance of a third circuit of the same type as that of the first circuit and in accordance with a next generation process and the performance correlation coefficient obtained in the second step, performance of a fourth circuit of the same type as that of the second circuit in accordance with the next generation process.

2. The method for predicting performance of an integrated circuit of claim 1, further comprising a fourth step of predicting the performance of the third circuit from a trend for performances of the first circuit and a circuit of the same type as that of the first circuit and in accordance with a different existing process generation from that of the first circuit,

wherein a predicted value for the performance of the third circuit which has been obtained in the fourth step is used in the third step.

3. The method for predicting performance of an integrated circuit of claim 1, wherein the second step includes a fifth step of predicting a performance correlation coefficient between the third and fourth circuits from a trend for performance correlation coefficients of different existing circuits which are the same types as those of the first and

second circuits, respectively, and

the performance correlation coefficient predicted in the fifth step is used in the third step.

4. The method for predicting performance of an integrated circuit of claim 1, wherein at least one of delay time, power consumption and chip area of each of the circuits is used as the circuit performance.

5. The method for predicting performance of an integrated circuit of claim 1, wherein performance of all or part of existing circuits are obtained using simulations, model equations or TCAD (Technology Computer Aided Design).

6. The method for predicting performance of an integrated circuit of claim 1, wherein performance of all or part of existing circuits are obtained using actual measurement.

7. A method for designing an integrated circuit, comprising the steps of:

generating a circuit library for a next generation process from prediction results obtained in the method for predicting performance of an integrated circuit of claim 1; and

performing circuit design based on the generated circuit library using the next generation process.

8. A method for predicting performance of an integrated circuit in an early stage of development, comprising:

a first step of obtaining performance of each of old circuits in accordance with

multiple existing generation processes; and

a second step of predicting performance of a new circuit of the same type as that of the old circuits and in accordance with a next generation process from a trend for performances of the old circuits of the different existing process generations.

9. The method for predicting performance of an integrated circuit of claim 8, wherein at least one of delay time, power consumption and chip area of each of the circuits is used as the circuit performance.

10. The method for predicting performance of an integrated circuit of claim 8, wherein performance of all or part of existing circuits are obtained using simulations, model equations or TCAD (Technology Computer Aided Design).

11. The method for predicting performance of an integrated circuit of claim 8, wherein performance of all or part of existing circuits are obtained using actual measurement.

12. A method for designing an integrated circuit, comprising the steps of:

generating a circuit library for a next generation process from prediction results obtained in the method for predicting performance of an integrated circuit of claim 8; and

performing circuit design based on the generated circuit library using the next generation process.